TS4231 Design Guidelines

The following document describes design practices that will help optimize the performance of TS4231 operation. Due to the high sensitivity and analog precision of TS4231, PCB layout and component selection can affect performance. The purpose of this guideline is to suggest best practices which will help to ensure optimal performance of TS4231.

1 Minimizing Differential Mode Noise:

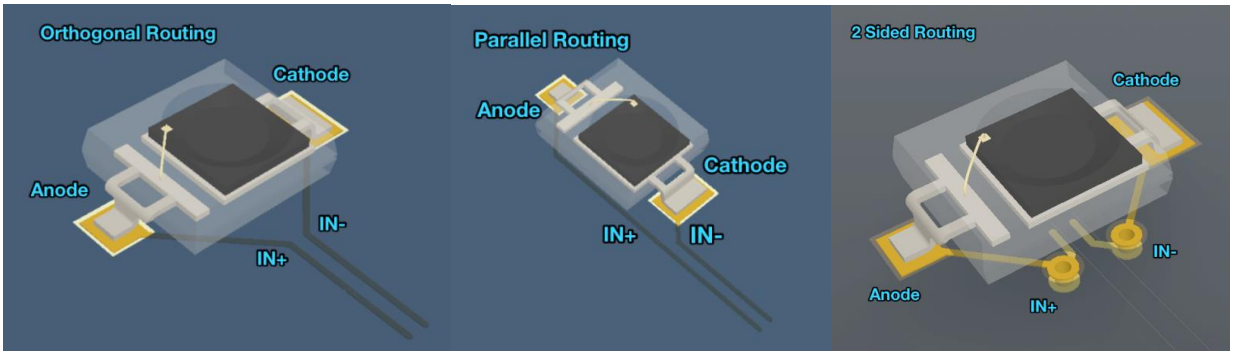
TS4231 features a differential input topology. This topology along with the careful design of the TS4231 internal circuit aims to have a high amount of Common Mode Rejection (CMR). This means that TS4231 is capable of rejecting noise and interference at the IN+ and IN- nodes so long it is within the supply voltage range and the noise is equally coupled to both the IN+ and IN- pins. This equal coupling of noise to both IN+ and IN- can be synonymous with “Common Mode”.

In the scenario where interference may couple disproportionally more to the IN+ node than the IN- node (or vice versa, more interference coupled to the IN- node than the IN+ node), this shall be referred to as “Differential Mode”. TS4231 is effective at rejecting Common Mode interference while Differential Mode Interference will be added or subtracted from the photo currents which are then amplified. TS4231 is designed to sense very small differential signal currents. Noise coupling, within the specified signal bandwidth, that is not common to both inputs will be amplified by the full gain of the receiver. Thus, it is very important to keep the scale of any differentially induced noise to be less than the level of signal that’s being detected.

A standard method in electrical design to prevent differential mode interference coupling is to layout the circuit in a symmetrical fashion where both the IN+ and IN- traces have the exact same effective length, shape and electrical characteristics. These characteristics include parasitic capacitance and inductance.

Often differential pair routing is used to minimize differential mode coupling. Differential Pair routing is recommended for TS4231 layouts however designers are explicitly required to have process control for maintaining a specific impedance value. More simply put, IN+ and IN- routes shall be of equal length, equal trace width and maintain an equal distance from one another as much as reasonable possible.

Given the package design of most BPW34S Photodiodes, the package itself is not symmetrical in design so it is not feasible to have a perfect design, rather the following images below demonstrate recommended methods for connecting a differential pair to BPW34S.

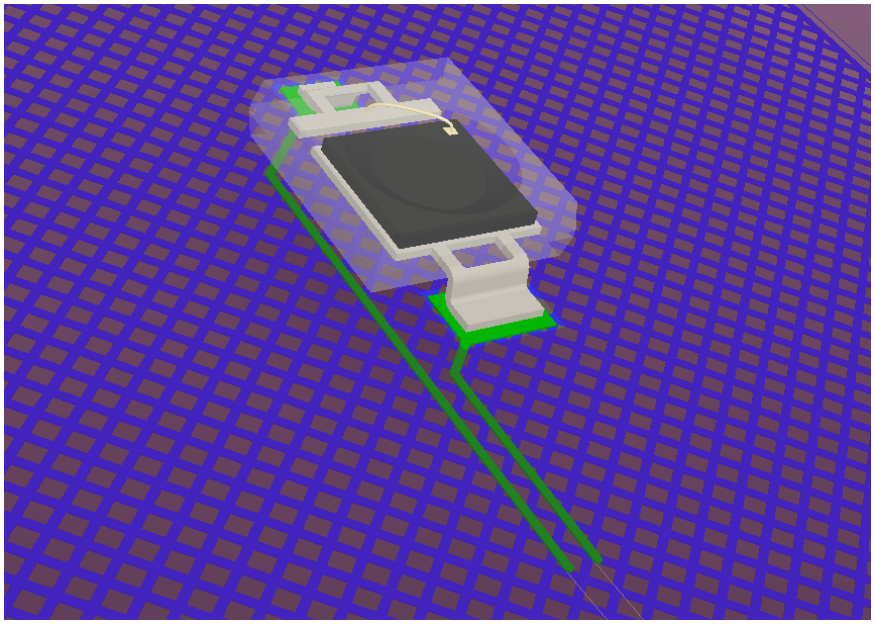


2 Minimizing Photodiode Parasitic Capacitance

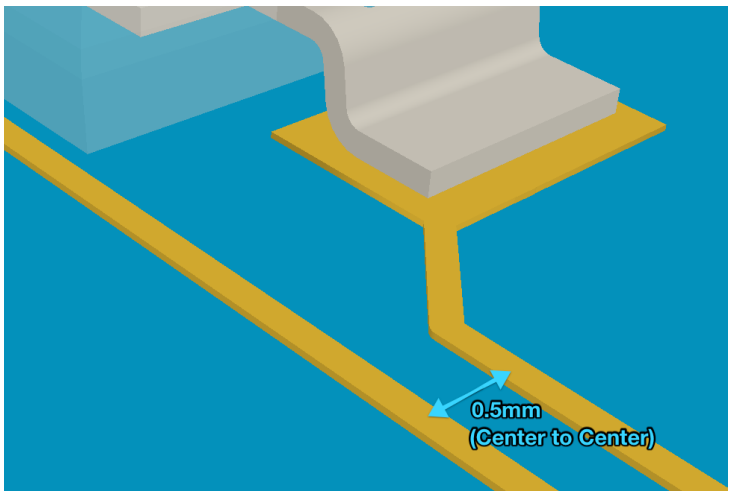
TS4231 is capable of detecting a very small amount AC current sinking through the DC biased Photodiode. These means that any capacitive path may shunt current away from the TS4231 effectively increasing attenuation and lowering device sensitivity. As a result, it is very important to reduce all forms of parasitic capacitance at the device's IN+ and IN- pins. This capacitance includes parasitic capacitance from IN+ to Ground, IN- to Ground as well as IN+ to IN-.

A first order way to think about parasitic capacitance is two parallel plates of metal separated by a thickness of dielectric. Capacitance increases when the surface area of the parallel plates increases. Capacitance also increases when the distance between the plates decreases.

Flex circuits are especially prone to higher parasitic capacitance because the dielectric materials tend to be very thin, perhaps only a few mils thick. To reduce this impact, it is recommended to use a crosshatched ground fill instead of solid copper. A crosshatched ground plane helps to lower capacitance by reducing the overlapping surface area of the ground plane copper and the adjacent traces. With cross hatching it is also recommended to maximize areas where the IN+ and IN- traces run perpendicular to the ground traces. The following is an example of a parallel routed Photodiode atop a crosshatched ground plane. The trace width of this ground plane is 6mil with a standard 20mil grid size.



In the case of IN+ to IN- parasitic capacitance, this is caused by edge to edge coupling between the IN+ and IN- traces. This capacitance is largely controlled by the spacing between these two routes. Due to the extremely thin plate area of the Copper trace thickness, this coupling can be greatly diminished with small changes to trace spacing. Since this requirement conflicts with the above requirements for symmetrical routing, it is recommended that a reasonable spacing between routes is 0.5mm:

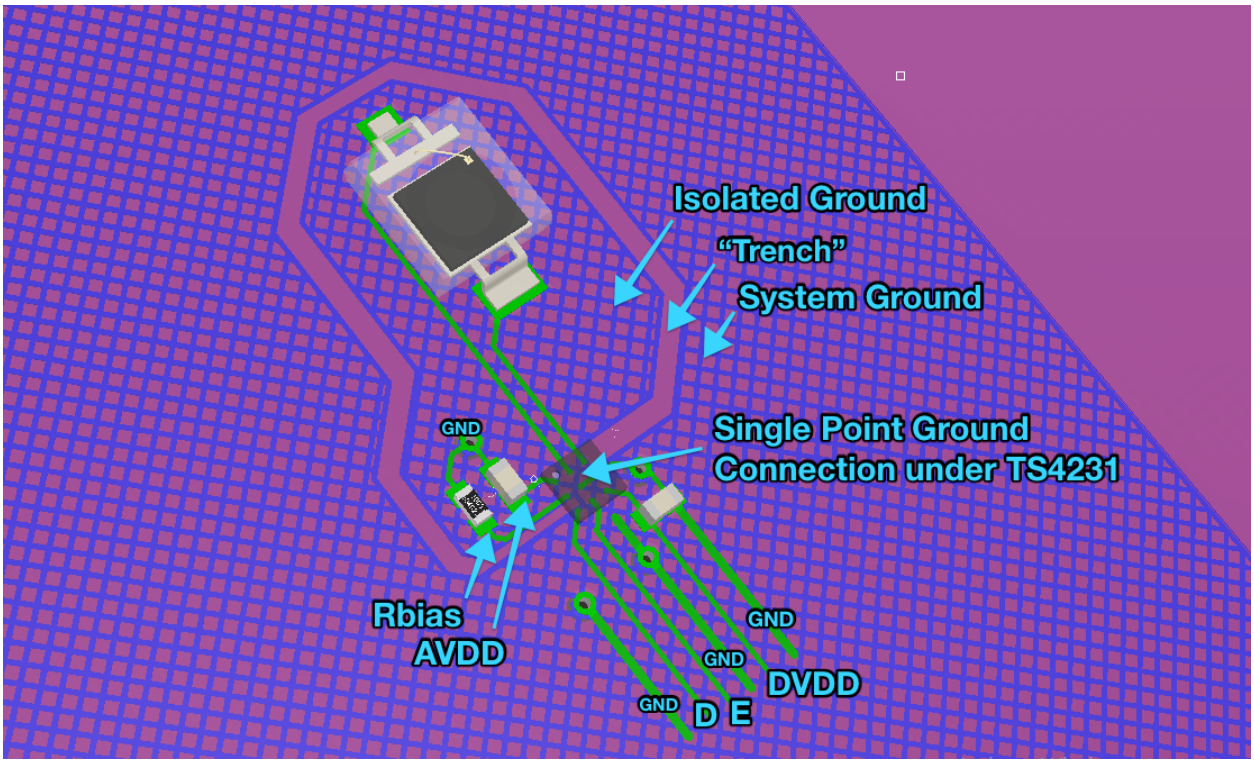


For all cases (flex and rigid PCBs), parasitic capacitance can be minimized by:

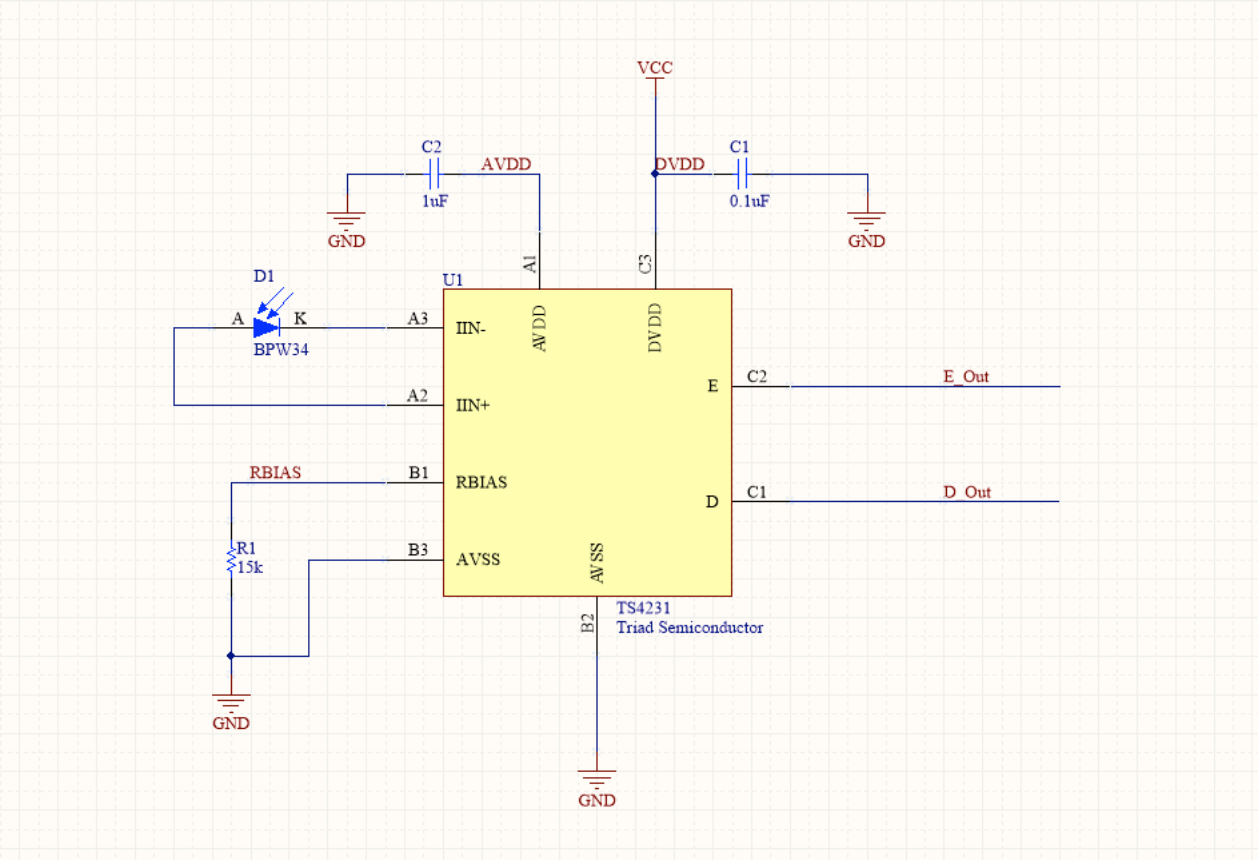
1. Using minimum trace width as defined by your PCB design rules, for example 6mil or 8mil trace width
2. For Dielectrics ~6mil or thinner (typically flex circuits), use of a cross hatched ground plane is recommended.
3. Spacing of IN+ and IN- about 0.5mm (center to center).

3 Ground fill Isolation

As described in Section 1, TS4231 has good performance in rejecting interference when it is coupled in the common mode. Another mechanism for interference coupling is through induced potentials caused by return currents circulating along paths in the ground plane. Due to this phenomena, it is recommended to “isolate” the ground plane in the analog region of the TS4231 layout to “steer” current away from sensitive nodes. This isolation is implemented with a “split” or “trench” that has a single point connection to the common ground plane for the rest of the PCB Design. The layout below demonstrates how you may practically implement ground fill isolation.



4 Recommended Bill of Materials



5 Power up

To minimize power up in rush current which charges up the supply bypass capacitors, DVDD ramp time should be between 300 µS and 1.5 mS.

6 Configure After Light Detected

Upon power up, communications and device configuration must be delayed until after the TS4231 initially detects signal, from the photodiode, which will be indicated via an active high detection pulse on pin D out. When awakening the device from configuration mode or from dynamic power savings sleep modes the TS4231 pins must be tri-stated within 70ns of wake up since the device will drive the output when the input signal is detected and the device may also detect based on wake up transients within first 50 µs of awakening. Once device is in Envelope plus Data Mode, the D pin is always driven by TS4231.

7 Debug and Probing

The IN+ and IN- inputs on the TS4231 are sensitive nodes that connect to a high-gain signal path. When attaching oscilloscope probes near the TS4231 on the D and E outputs sometimes you will see extra pulses on the D output. These pulses should not exist but they are often due to noise coupling through the scope probe to the TS4231 input. Scope probes add parasitics and create noise coupling loops.

Pulses on the D output of the TS4231 are valid only when the E output is also asserted. Pulses on the D output can be ignored when E is not asserted.

Performance will be much improved without scope probes connected to the output of the TS4231. This complicates debugging but the TS4231 digital outputs can be monitored downstream via SteamVR HDK tools or in custom hardware within your FPGA or microprocessor code.

If you must probe near the TS4231, we recommend using an active differential probe or soldering a 30-gauge wire to the probe point and twisting with ground wire to minimize the probe loop area.

Revision History

Revision	Modifications	Modification Date
A	Initial design guidelines release	15 Aug 2017

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