1 Features

- **Light to Digital Converter with integrated IR photodiode for SteamVR™ Tracking**
- Low power for battery operated applications
- Deep Sleep Mode
- Compatible with all versions of SteamVR™
- Convert infrared light pulses to digital envelope pulses used to track position
- Convert infrared light pulses to digital pulses that follow the optical carrier
- 1MHz to 10MHz optical carrier frequencies
- 50Hz/60Hz ambient noise rejection
- Two-wire control bus shares E/D pins
    - Sleep command
    - Configuration
- DVDD: 3.3V
- Small 6mm x 3.5mm package size simplifies industrial design of tracked objects

2 Applications

- SteamVR Tracking Applications
- Room-scale Virtual Reality Tracking
- Virtual Reality Controllers
- Tracking of Physical Objects in VR
- Adding SteamVR Tracking to VR Head Mounted Displays
- Robotics Positioning
- Active Infrared Detectors
- Photoelectric Detectors
- Volumetric Entertainment Systems
- Optical Ranging
- Optical Detection
- Free-Space Optical Communication

3 Description

Triad Semiconductor's TS4112 enables cost effective deployment of Valve Corporation's SteamVR™ Tracking System. With an integrated photodiode and no external components required, the TS4112 provides a low-cost, area-efficient solution for a complete IR to digital converter solution. The TS4112 converts infrared light pulses into position-indicating digital envelope signals and includes a digital output data pin that is a representation of the optical carrier waveform applied to the photodiode. The TS4112 includes circuits for photodiode biasing and provides high gain, noise filtering and envelope detection of a pulsed IR light sources. The Envelope output of the TS4112 is a digital signal that tracks the envelope of the amplitude modulated (OOK or ASK) infrared light that is incident on the photodiode. The data output is a digital signal that tracks the modulated light input. The TS4112 is configured by a two-wire bus that shares the E/D pins of the device.

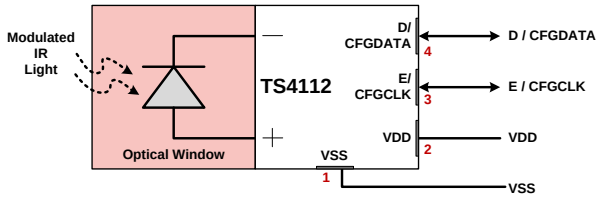


Figure 1 – TS4112 Simplified Application Circuit

Figure 2 – 6mm x 3.5mm Opto-Electronic Package

4 Device Overview

The TS4112 is a mixed-signal device for receiving modulated near infrared light. The TS4112 is ideal for use in optical position tracking applications such as Valve Software Corporation's SteamVR™ Tracking. The TS4112 package is a 6mm long, 3.5mm wide, 0.8mm tall plastic encapsulated package with an infrared clear optical window and generous pad spacing. The mechanical design of the TS4112's package greatly simplifies industrial design and allows for low-density, low-cost flex printed circuit (FPC) manufacturing.

The TS4112 provides pulse detection circuitry for use in room scale tracking/positioning for virtual reality gaming and other applications which require millimeter position accuracy. The internal photodiode is connected to the inputs of a differential transimpedance amplifier (TIA). The output of the differential TIA is followed by filtering and gain blocks to limit noise before the signal drives an envelope detector and data slicer to generate the output signals. Figure 3 shows the block diagram of the TS4112.

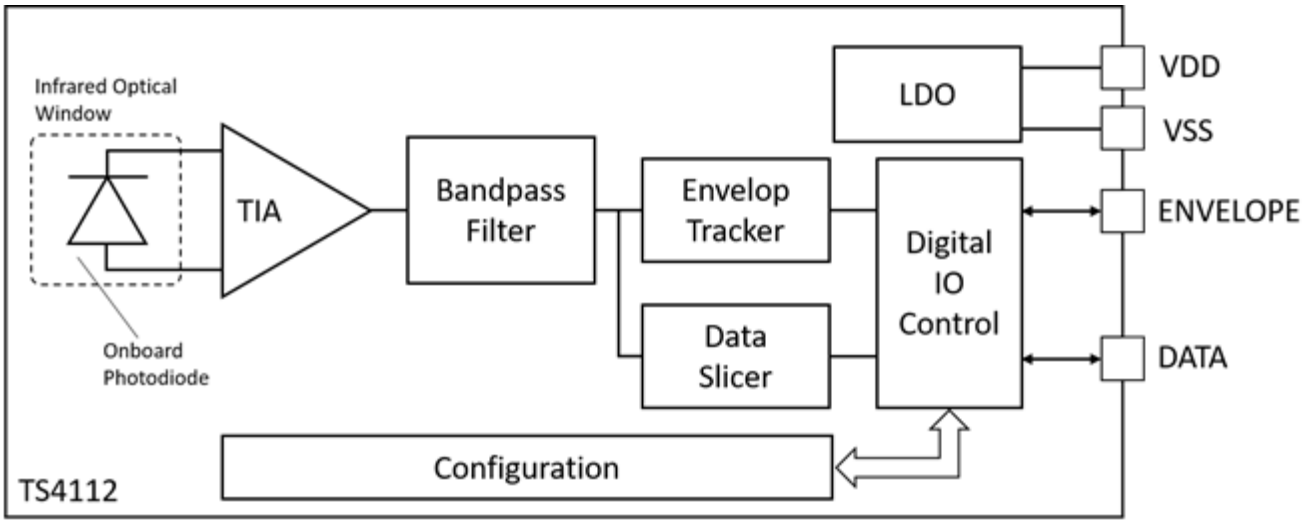


Figure 3: TS4112 Basic Block Diagram

5 Signal Path

5.1 Integrated Photodiode

The TS4112 includes an integrated photodiode with 7.5mm^2 active area. The photodiode is covered with an optical window that filters out visible light allowing the TS4112 to detect small infrared signals in bright indoor and outdoor sunlight conditions.

5.2 TIA & Filter Amplifier

The TIA is designed to amplify differential current pulses from the photodiode. This TIA supports fast pulses and is targeted at receiving optical signals that are modulated in the 1MHz to 10MHz range.

5.3 Envelope and Data Detectors

The Envelope Detector is triggered by an amplified and filtered signal crossing a configured threshold. The Envelope output is asserted during detection of light pulses incident on the photodiode. The data detector is implemented using a comparator with controlled hysteresis. The Data pin low time is qualified with an internal one-shot and is forced to return low if the low duration exceeds a 600-900ns timeout. See Figure 4.

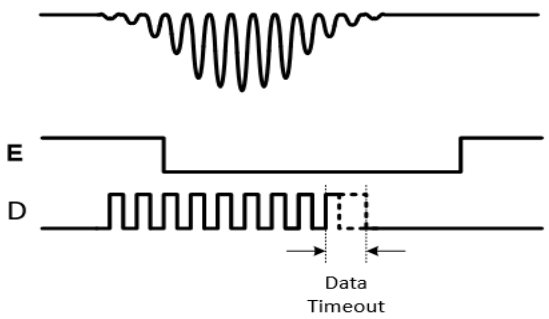


Figure 4: Output Waveforms for Modulated IR light with Gaussian Envelope

6 Digital Control Interface

The TS4112 provides a digital control interface (see Figure 5) that can be controlled by the Valve SteamVR Tracking HDK FPGA (alternative FPGA or microprocessor based control interfaces are available). After device power on, the SteamVR Tracking HDK communicates with the TS4112 over the E and D pins to configure the device. Waiting for initial IR light detection is not required for TS4112. After power supply stabilization, the SteamVR Tracking HDK communicates with the TS4112 over the E and D pins to configure the device. After being configured, the device will be in normal watch mode looking for modulated IR light. When the device's photodiode is exposed to modulated IR light within the frequency range of the device, the envelope output is asserted on the E pin and the carrier data is output on the D pin.

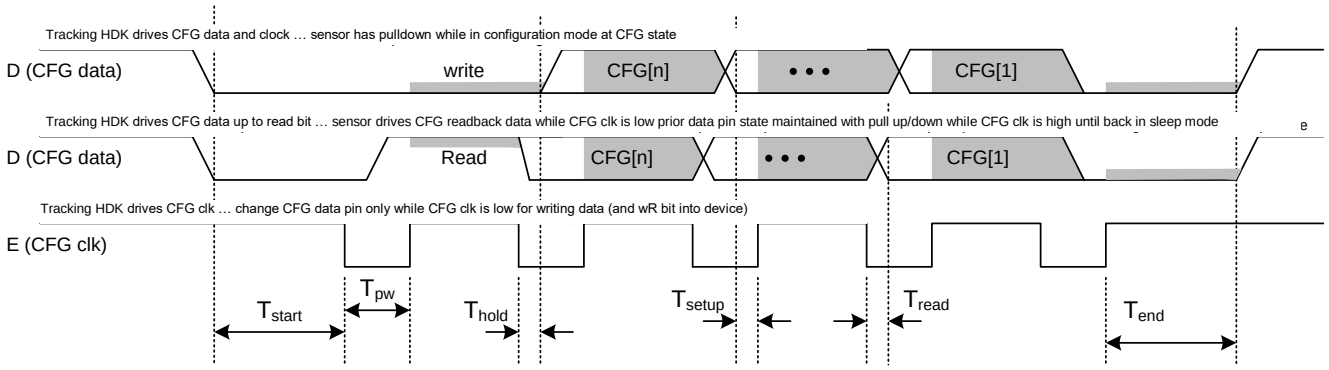


Figure 5: Configuration Interface Timing

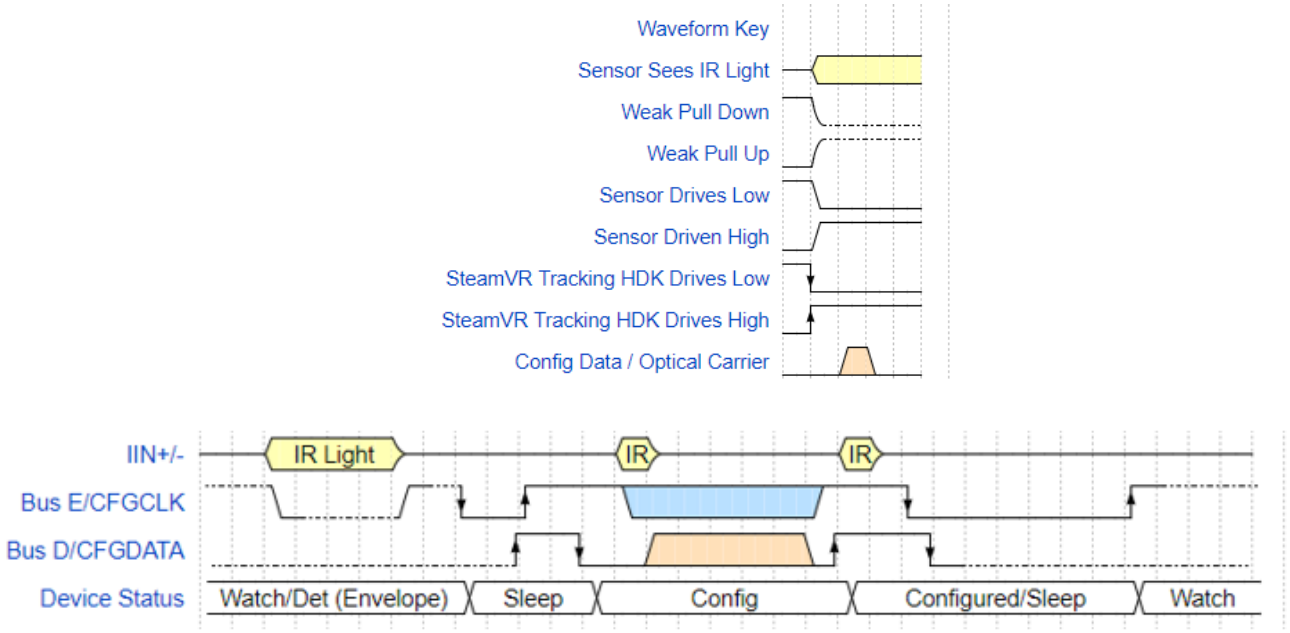


Figure 6: TS4112 powers up Un-configured then the SteamVR Tracking HDK configures the device

6.1 Sleep & Deep Sleep Mode

While in watch mode, the Tracking HDK may put TS4112 into Sleep mode or Deep Sleep mode by driving the E Pin low. To return to Watch mode, the Tracking HDK will drive the E Pin high and then quickly transition to a high impedance input.

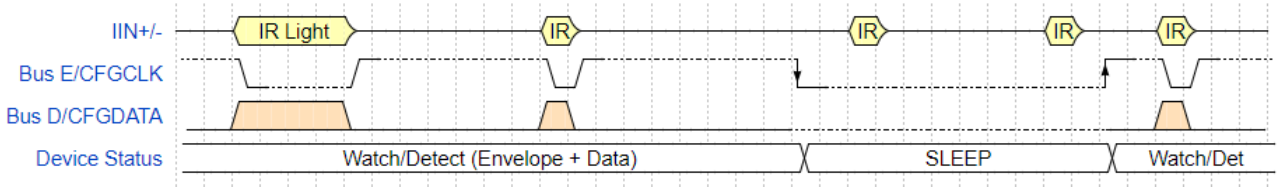


Figure 7: Sleep Timing

6.2 Enabling Deep Sleep Mode

In addition to Sleep mode, TS4112 also supports a Deep Sleep mode. Deep sleep mode has a significantly lower power consumption but requires additional time to transition from sleep to the watch/detect state. The specifications for Sleep and Deep Sleep performance are listed in Section 7.4. The configuration words listed in section 6.3 describe how to configure TS4112 to use Sleep or Deep Sleep mode.

6.3 Configuration Words

The following table describes the acceptable configuration words for TS4112. These 14 bit configurations can be written to the device as described in section 6.1.

Configuration Word	Mode
0x0499	Envelope and Data Enabled with Sleep Mode (Faster Wake up)
0x049A	Envelope and Data Enabled with Deep Sleep Mode (Lower Current)

7 Performance Characteristics

7.1 Absolute Maximum Ratings

Parameter[1][2]	Notes/Conditions	MIN	MAX	units
DVDD			3.6	V
Digital Input Voltage		-0.3	3.6	V
Junction Temperature T_{JMAX}	Maximum junction temperature		150	°C
Storage Temperature, T_{STOR}	Storage temperature range	-40	150	°C
Soldering Information: infrared or convection (30 sec)	Peak body temperature (reflow)		260	°C

(1) All Voltages are specified with respect to GND = 0Vdc

(2) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

7.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Parameter	Notes/Conditions	MIN	TYP	MAX	units
DVDD	Supply voltage	3.0	3.3	3.6	V
T_{AMB}[1]	Operating temperature range	0		85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, Θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is PD = $(T_{J(MAX)} - T_{AMB})/ \Theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board

7.3 Thermal Information

Parameter	Thermal Metric		units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W

7.4 Electrical Characteristics

Operating conditions: DVDD = 3.3V, T_{AMB} = 25 °C unless otherwise noted(1).

Parameter	Notes/Conditions		MIN(2)	TYP(3)	MAX(2)	units
Power Supply						
I_{VDD}	Operating current			2.5	3.5	mA
Sleep_I_{VDD}	Sleep mode current			0.5	0.7	mA
Deep Sleep_I_{VDD}	Deep Sleep mode current				0.15	mA
Digital IO						
V_{IL}	Input Low Voltage				0.25 * VDD	V
V_{IH}	Input High Voltage		0.75 * VDD			V
V_{OL}	Output Low Voltage	@ 2 mA load			0.1 * VDD	V
V_{OH}	Output High Voltage	@ 2 mA load	0.9 * VDD			V
I_{PU}	Output Pullup Current		70	105	140	µA
I_{PD}	Output Pulldown Current		70	105	140	µA
Rise(2)	10/90% Output Rise Time	Slew rate limited 5-20pF load	7		36	nS
Fall	10/90% Output Fall Time	Slew rate limited 5-20pF load	7		36	nS
T_{start}			80			ns
T_{pw}			80			ns
T_{setup}			30			ns
T_{hold}			30			ns
T_{end}			80			ns
T_{read}					75	ns
System						
Freq	Input pulse frequency	HiPass – LoPass 3dB corners	1.5		10	MHz
I_{INDET}	In band detection input current level (max gain)	w/ App Schematic			1.0	µA
I_{INMAX}	In band input current level max	w/ App Schematic			100	µA
$Sleep_{RCVRY}$	Sleep Mode Recovery timing E and D outputs should be ignored during recovery time	10 – 90% on I_{VDD}			50	µS
$Sleep_{PDN}$	Sleep Mode Power Down timing	10 – 90% on I_{VDD}			50	µS
$DeepSleep_{RCVRY}$	Deep Sleep Mode Recovery timing E and D outputs should be ignored during recovery time	10 – 90% on I_{VDD}			200	µS
REJ_{50KHz}	50KHz Rejection	@ filter output	40			dB

(1) Electrical Characteristic values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested
(2) Rise and Fall Times are ensured by design and not production tested.
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material

8 Applications and Design Considerations

8.1 Application Schematic

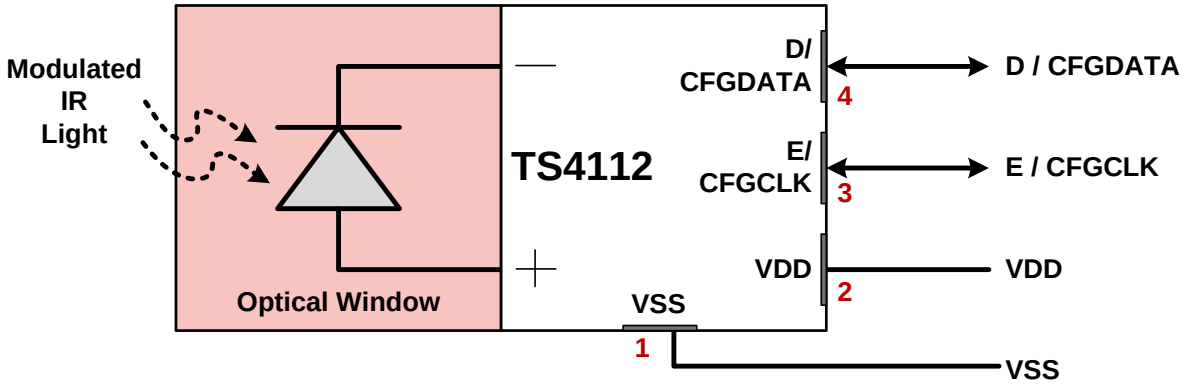


Figure 8: TS4112 Application Schematic

8.2 Power Supply Recommendations

The TS4112 was designed to be operated from a 3.3V power supply. The voltage range for DVDD is shown in *Recommended Operating Conditions*. Power supply accuracy of 10% or better is advised.

8.3 Layout Recommendations

Do not connect pins 5, 6, nor 7 to ground. Any vias placed underneath the part should be tented to prevent the possibility of shorting between exposed pads. The photodiode cathode of pin 7 should not be electrically connected to any other signal on the board. Pin 7 is electrically connected to the cathode of the internal photodiode and should be isolated from other electrical connections. Pin 7 needs to be soldered to the pads as shown in **Figure 12**, the soldered connection will serve as a mechanical connection to the PCB or FPC.

9 Part Packaging Information

9.1 Package Drawing

The TS4112 – Light to Digital Converter is packaged as a 6mm x 3.5mm x 0.8mm overmolded package with optical window. Figure 11 shows the package configuration.

9.2 Date Code

The manufacturing date code is printed on the package as described in this section of the datasheet. The manufacturing code has the format of XXXX YY where XXXX is the lot code, YY is the plant code.

10 Pin List

#	Pin Name	Pin Type	Pin Description
1	VSS	Supply	Ground
2	VDD	Supply	Power
3	E	Digital I/O	Envelope Output / Configuration Clock I/O
4	D	Digital I/O	Data Output / Configuration Data I/O
5	EP1	Mechanical	Exposed pads. Do not provide a corresponding landing pad on the printed circuit board. These exposed pads on the IC should NOT be electrically nor mechanically connected to the PCB.
6	EP2	Mechanical	
7	PD	Mechanical	Exposed pad. This pad is used to mechanically attach the IC to the printed circuit board. This pad should be soldered to the PCB with the landing pads shown in the Recommended Footprint Diagram (**Figure 12**). This pad should NOT be electrically connected to any other circuit.

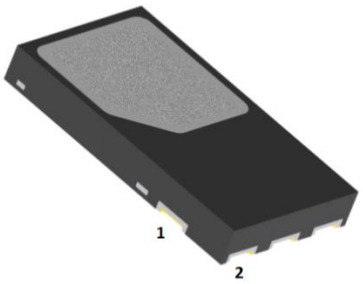


Figure 9 TS4112 Pin 1 Indication

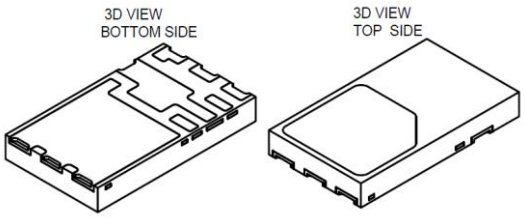


Figure 10 - 3D Package View

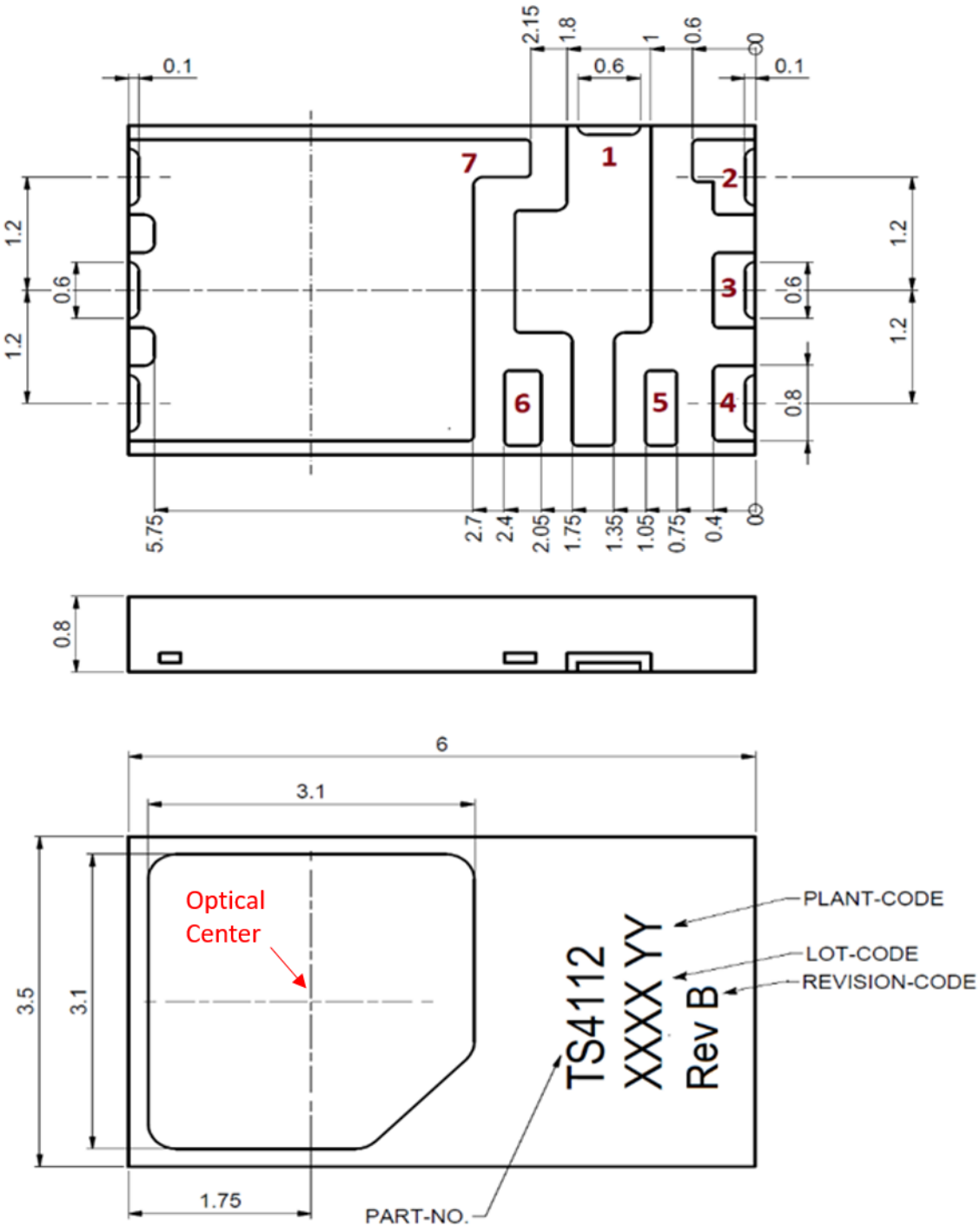


Figure 11 - TS4112 Mechanical Dimensions

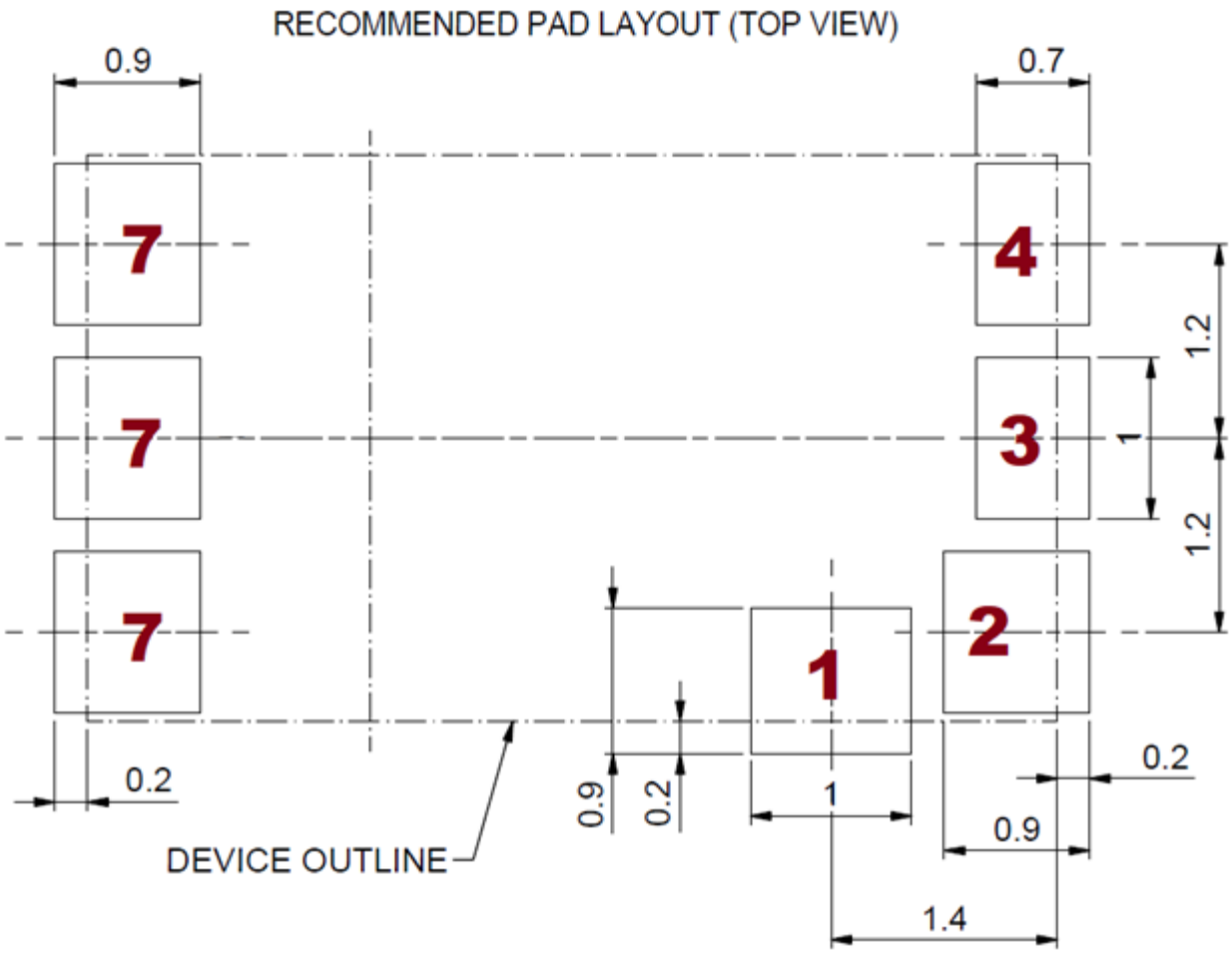
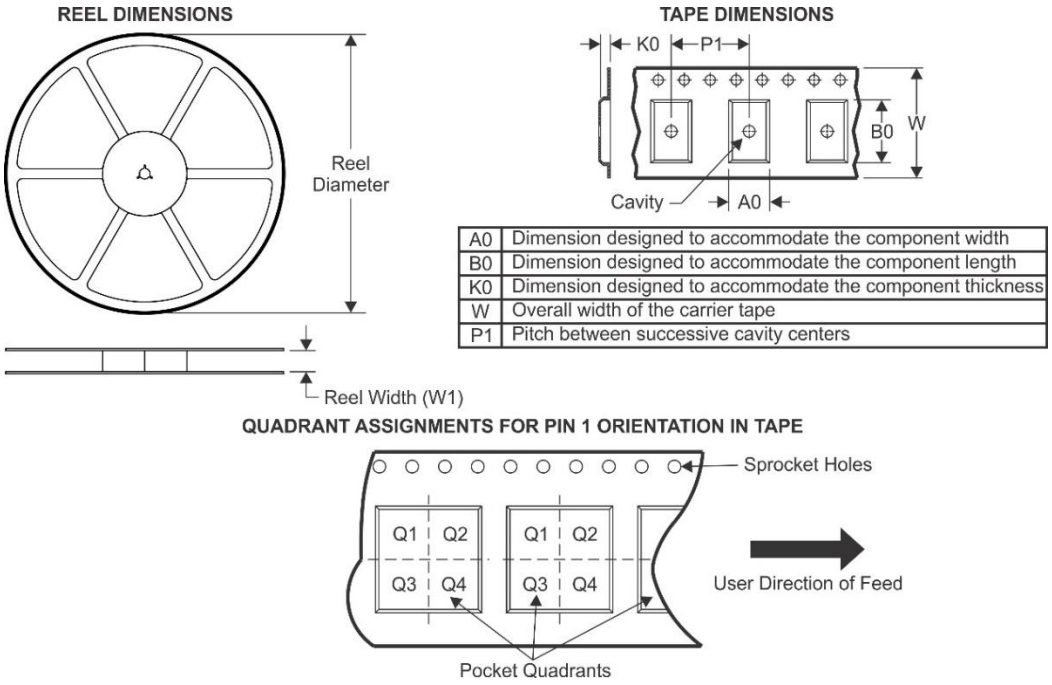


Figure 12 TS4112 Recommended Footprint

11 Tape and Reel Packaging

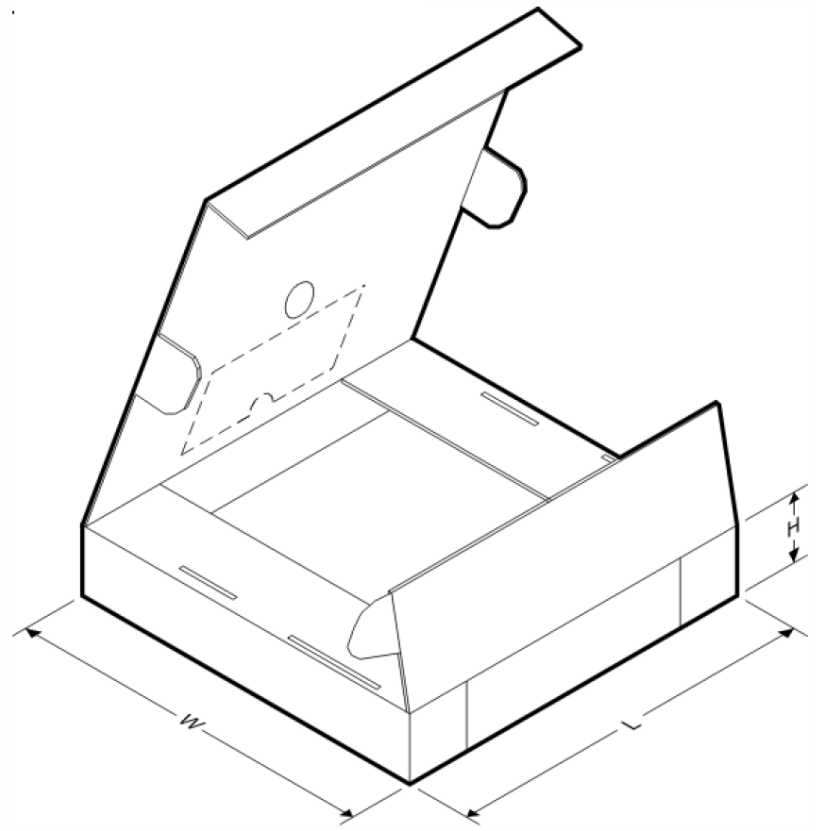
11.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pads	Qty / Reel	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
TS4112	QFN	4	1000	178.0	20	5	7	1.2	7.75	16.1	Q3

11.2 Tape and Reel Box Dimensions



Device	Package Type	Qty / Reel	Length (mm)	Width (mm)	Height (mm)
TS4112	QFN	1000	TBD	TBD	TBD

Note: All dimensions are nominal

12 Mechanical, Packaging and Handling Information

Device	Package Type	Pads	Package Qty	RoHS Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Storage Temp (°C)	Device Marking
TS4112	QFN	4	1000	RoHS & no Sb/Br	TBD	TBD	0 to 85	-40 to 150	TS4112

12.1 Electrostatic Discharge Caution

TS4112 is an ESD sensitive device with an HBM rating of Class 2 (2,000V) per JS-001-2017. The device should be placed in conductive foam during storage or handling to prevent damage due to electrostatic discharge. Refer to JESD625 for handling precautions.

12.2 MSL

TS4112 is an MSL 4 device per J-STD-020. Refer to J-STD-033 for specific handling requirements and conditions.

12.3 Shelf Life

Shelf life is 12 months as per J-STD-033. Refer to J-STD-033 for additional shelf life information.

13 RoHS

TS4112 fully complies with the RoHS Directive 002/95/EC requirements without exemption and is Halogen-Free as defined by IEC 61249-2-21.

Revision History

Revision	Modifications	Modification Date
A	Initial release Rev A Datasheet	16 August 2018
B	Added Section 10.1 with recommended design and paste deposition profile	10 June 2019
C	Updated package dimensions and diagrams throughout document from updated pad layout and addition of wettable flanks.	18 June 2019
D	Corrected typo in pin table for E and D pins	5 July 2019
E	Corrected typo in table 10. AVSS and DVDD swapped	5 July 2019
F	Update to layout recommendation and correction to diagram references	8 July 2019
G	Added optical center to mechanical drawing, Indicated MSL4, updated Pin List information regarding exposed pads and pad 7.	1 October 2019

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Triad Semiconductor designs and manufactures analog and mixed signal integrated circuits. Founded in 2002, Triad provides custom IC, ASSP and standard product solutions to customers in all major markets.

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