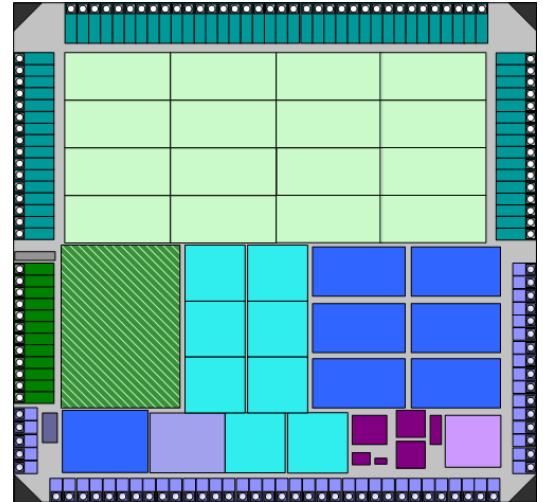


VCA-4 – Low-Power, Low-Noise

The VCA-4 combines very low power, low-noise analog resource with low-power digital and EEPROM memory resources on a single ASIC array to address a wide range of precision portable applications. The VCA-4 contains 24,000 ASIC gates, 8Kbyte of non-volatile EEPROM memory, and 16Kbits of embedded SRAM. The A-4 array is optimized for low-noise sensor interfacing, high resolution data conversion, and the low-power operation need for medical, consumer, and industrial battery powered sensor interfaces. The A-4's internal PLL enables operation from low cost 32KHz "watch" crystals and supports operation from 32KHz to 2MHz.

The VCA-4 utilizes a single mask layer to change analog, digital, and memory circuits resulting in:

- Reduced NRE Charges
- Rapid Time to Prototypes
- Fabrication Time in Weeks not Months
- Reduced Risk



Resources

Digital

- **24,000 Logic Gates**
- 32 Kbits of 1-Port SRAM
- 4Kx16 EEPROM, 20-Year Retention
- 48 Configurable Digital I/O
- 3.3V Digital Power
- 32KHz to 2MHz PLL

Analog

- **Low-Power, Low-Noise**
- 3.3V Analog
- 6 Low Power Fully Differential Analog Tiles
- 8 Low Power Low Noise Single Ended Analog Tiles
- 12 Wideband/Low Noise Op-amp Tiles
- 1 Low Power Bias Generators
- High Resistance Tile
- 2 10-bit Digital Potentiometers
- Temperature Sensor

Applications

- Universal Sensor Processor
- Smart Sensor Interface (IEEE1451.4)
- Mixed Signal 8051
- Remote Data Logger
- Portable Medical Device
- Battery Powered Circuits
- Capacitive Sensor Interface
- Semi-Passive RFID Transponder (Tag)
- Vibration Sensor
- pH Meter

Table 1 - VCA-4 Resources

Digital Resources

- **24,000 Logic Gates**
 - 16 Logic Tiles – LT2K-1P-1500
 - 16 Distributed SRAMs
 - 64 x32 1-Port RAM (2048-bits)
 - 32,768 bits total distributed RAM
 - **Non-Volatile Memory**
 - 4K x 16 EEPROM
 - Verilog Wrappers for 8-bit interfaces
 - 20 Year Data Retention
 - 100K Cycle Write Endurance
 - Byte & Page Mode Write Operations
 - Integrated Charge Pump & Control
- **48 Digital I/O**
 - Via Configurable Options
 - Input, Output, Bidirectional
 - Slew Rate Control
 - Pull-Up, Pull Down
 - Drive Strength
 - 2 Digital VDD Pads
 - 2 Digital VSS Pads
- **32KHz to 2MHz PLL**

Analog Resources

- **Low-Power, Low-Noise op-amps for precision sensor acquisition applications.**
- **6 Low Power Low Noise Single Ended Analog Tiles**

LP-LN-A-TILE Resources

- 2 Low Power, Low Noise Single Ended OTA/Op-Amps
- 1MHz Gain Bandwidth
- Capacitor Array
- Resistor Array
- Transistor Array
- Switch Array
- Logic Array
- Configurable Bias Generator

▪ 6 Low Power Fully Differential Analog Tiles

LP-FD-A-TILE Resources

- 2 Fully Differential OTA/Op-Amps
- 4MHz Gain Bandwidth
- Differential Capacitor Array
- Differential Resistor Array
- Differential Transistor Array
- Differential Switch Array
- Logic Array
- Configurable Bias Generator

Support for chopper-stabilized and correlated double sampling architectures to achieve very low offsets and high resolution with inherently low input referred noise.

▪ Low Power Bias Generator

▪ High Resistance Tile

▪ Digital to Analog Converters

- 2 DP1001 – 10-bit Digital Potentiometers

Analog to Digital Converters can be created as soft-IP using the OTA/Op-Amps, switches, and capacitors within the array. Sigma-Delta and Successive Approximation converters with resolutions up to 14-bits and sample rates up to 1MSPS are realizable.

▪ Temperature Sensor

▪ Miscellaneous Analog

- Voltage Reference Network

▪ 52 Analog I/O

- Via Configurable Options
 - 1500 50, 0 Ohm pad resistance
 - 4 Analog VDD Pads
 - 4 Analog VSS Pads

